



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/072,212

02/07/2002

Anshuman Nayak

X-2417 US

2745

24309 7590 10/17/2007

XILINX, INC  
ATTN: LEGAL DEPARTMENT  
2100 LOGIC DR  
SAN JOSE, CA 95124

EXAMINER

WOOD, WILLIAM H

ART UNIT

PAPER NUMBER

2193

MAIL DATE

DELIVERY MODE

10/17/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/072,212

Applicant(s)

NAYAK ET AL.

Examiner

William H. Wood

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 23 July 2007.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 and 21-39 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1 and 21-39 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

Claims 1 and 21-39 are pending and have been examined.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 21-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bowen** (US Publication 2003/0105620 A1) in view of **Smith et al.**, "An Architecture Design and Assessment System for Software/Hardware Codesign". Paragraph 9 of the office action mailed 10 April 2006 contains a detailed rejection of claims 21-39.

#### Claim 1

**Bowen** disclosed a computer-automated method for electronic design specification comprising:

obtaining a target architecture (*paragraph 0144, "Handel-C is a programming language that enables ... to target directly FPGAs"*);

specifying at least one resource or functionality for the target architecture using at least one construct in a Resource Description Language (RDL) to produce an RDL description (*paragraph 0145, lines 6-9 and figure 84*);

generating an intermediate representation from the RDL description (*paragraph 0268, "compiler creates a file which in turn compiled", internals of the first compiler*);

traversing the intermediate graph representation (*paragraph 0268, "creates a file which in turn compiled ... using Microsoft Visual C++"*); and **Bowen** did not explicitly state invoking results of the traversing step using a high-level synthesis compiler to generate a functionality graph and resource graph for the target architecture. **Smith** demonstrated that it was known at the time of invention to produce functionality graph (page 421, right column, section "Representing Software with Software Graph") and resource graph (page 422, left column, section "Representing Hardware with a Hardware Resource Graph"). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the hardware architecture program development of **Bowen** with functionality and resource graphs as found in **Smith's** teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to make use of tools (graphs) for a comprehensive representation of a system (page 421, right column, "directed graphs can be used to represent systems at various levels of the hierarchy, and subgraphs can be used to create a unified description of the entire hierarchy").

***Response to Arguments***

3. Applicant's arguments filed 23 July 2007 have been fully considered but they are not persuasive. Applicant argues the combination of **Bowen** and **Smith** does not disclose invoking results of traversing an intermediate graph representation using a high-level synthesis compiler to generate a functionality graph and resource graphs for the target architecture (Remarks: page 7, second paragraph).

As previously indicated, **Bowen** discloses generating an intermediate graph representation from the RDL description (paragraph 0268, "compiler creates a file which in turn compiled", internals of the first compiler) and traversing the intermediate graph representation. The compiler of **Bowen** internally creates a graph and further produces a file. **Bowen** fails to explicitly state the invoking results of the traversing step by a compiler to generate the graphs as claimed. However, **Smith** discloses the graphs and provides motivation (page 421, right column, section "Representing Software with Software Graph"; page 422, left column, section "Representing Hardware with a Hardware Resource Graph"; and page 421, right column, "directed graphs can be used to represent systems at various levels of the hierarchy, and subgraphs can be used to create a unified description of the entire hierarchy"), as previously indicated, for enabling the compiler of **Bowen** to invoke the results for generating the graphs. In view of this, Applicant's arguments are not

persuasive as **Bowen** and **Smith** combined demonstrate the claim limitation in question. Having addressed Applicant's concerns the rejections are maintained as above indicated.

### ***Conclusion***

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

### ***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)-272-3736. The examiner can normally be reached 10:00am - 4:00pm Monday thru Friday.

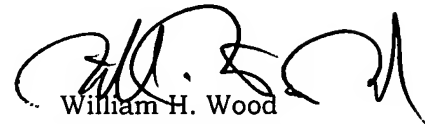
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)-272-3756. The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

Art Unit: 2193

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR systems, see <http://pair-direct.uspto.gov>. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.



William H. Wood  
Patent Examiner  
AU 2193  
October 12, 2007